Amendments to the Specification:

Please replace the paragraph at page 5, lines 21-22 with the following amended paragraph:

FIG. 2 shows a circuit diagram illustrating a second embodiment of the sense amplifier having ~~an asynchronous~~ a synchronous reset capability according to the present invention.

Please replace the paragraph at page 6, lines14-23 with the following amended paragraph:

The first controller 15 is connected to the first sense-amplifying unit 11 and sets the signal of the first output node O1 to logic "high" in response to a reset signal RESET and an inverted reset signal /RESET. That is, the first controller 15 resets the final output signal OUT-H to logic "low". The second controller 17 is connected to the second sense-amplifying unit 13 and ~~sets~~resets the signal of the second output node O2 to logic "low" in response to the reset signal RESET and the inverted reset signal /RESET. That is, the second controller 17 sets the complementary final output signal OUT_L to logic "high". The current source 19 is connected to the first sense-amplifying unit 11, the second sense-amplifying unit 13, the first controller 15, and the second controller 17 and responds to the clock signal CLK.